IN THE CLAIMS:

Kindly amend the claims, as follows:

1. (Amended) A signal processing apparatus comprising:

an input circuit to receive an input signal;

~~a feedforward equalizer comprising~~ a high-pass filter ~~and~~ responsive to said input circuit; and

a decision feedback equalizer comprising:

a decision circuit directly responsive to said ~~feed forward equalizer~~ high-pass filter; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

2. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said high-pass filter has a low cutoff frequency.

3. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 2, wherein said high-pass filter has a flat response.

4. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said high-pass filter has high attenuation at low frequency.

5. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said high-pass filter has high attenuation at low frequencies.

6. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 5, wherein the high attenuation is at least 20 db.

7. (Amended) ~~A signal processing circuit according to Claim 1~~ A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a first finite impulse response filter (FIR); and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

8. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 7, wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.

9. (Amended) ~~A signal processing circuit according to Claim 8~~ A signal processing apparatus, comprising:

an input circuit to receive an input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a first finite impulse response filter (FIR),

wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI,

wherein each tap of said first FIR filter has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$$-1 << W_1, \ldots W_n << 0; \text{ and}$$

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

10. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said input circuit comprises an analog to digital converter.

11. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said decision circuit comprises a threshold circuit.

12. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said decision circuit comprises a Viterbi detector.

13. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 8, further comprising ~~a~~ an first adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering postcursor ISI.

14. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 13, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

15. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 13, wherein said ~~first~~ adaptive control circuit is operable only during signal acquisition.

16. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 1, wherein said feedback filter comprises a second finite impulse response filter (FIR).

17. (Amended) A signal processing ~~circuit~~ apparatus according to Claim ~~15~~ 16, further comprising ~~a~~ an second adaptive control circuit to adapt taps of said second FIR filter.

18. (Amended) A signal processing apparatus comprising:

input means for receiving an input signal;

~~feedforward equalizer means for feedforward equalizing by~~ high-pass filtering means for filtering the input signal received by said input means; and

decision feedback equalizer means comprising: → see claim 8

decision means directly responsive to said high-pass filtering means for recovering data from an output of said ~~feedforward equalizer~~ high-pass filtering means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

19. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedforward equalizer means has a low cutoff frequency.

20. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 19, wherein said feedforward equalizer means has a flat response.

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21. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedforward equalizer means has high attenuation at low frequency.

22. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedforward equalizer means has high attenuation at low frequencies.

23. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedforward equalizer means shortens a length of postcursor inter-symbol interference.

24. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedforward equalizer means attenuates any DC noise.

25. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedforward equalizer means attenuates baseline wander.

26. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 22, wherein the high attenuation is at least 20 db.

27. (Amended) ~~A signal processing circuit according to Claim 18~~ A signal processing apparatus comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

28. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 27, wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.

29. (Amended) ~~A signal processing apparatus according to Claim 28~~ A signal processing apparatus, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal,

wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI,

wherein each tap of said ~~first~~ FIR filter means has a corresponding coefficient W as follows:

W_0 = unity

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$-1 << W_1, \ldots W_n << 0$; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

30. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

31. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said decision means comprises a threshold circuit.

32. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said decision means comprises a Viterbi detector.

33. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 28, further comprising ~~a first~~ an adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering postcursor ISI.

34. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

35. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 33, wherein said first adaptive control means is operable only during signal acquisition.

36. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 18, wherein said feedback filter means comprises a second finite impulse response filter (FIR) means for filtering the output of said decision means.

37. (Amended) A signal processing ~~circuit~~ apparatus according to Claim 36, further comprising ~~a~~ an second adaptive control means for adapting taps of said second FIR means.

38. (Amended) An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

~~a feedforward equalizer comprising~~ a high-pass filter ~~and~~ responsive to said input circuit; and

a decision feedback equalizer comprising:

a decision circuit directly responsive to said ~~feed forward equalizer~~ high-pass filter; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

39. (Original) An Ethernet transceiver according to Claim 38, wherein said high-pass filter has a low cutoff frequency.

40. (Original) An Ethernet transceiver according to Claim 39, wherein said high-pass filter has a flat response.

41. (Original) An Ethernet transceiver according to Claim 38, wherein said high-

pass filter has high attenuation at low frequency.

42. (Original) An Ethernet transceiver according to Claim 38, wherein said high-pass filter has high attenuation at low frequencies.

43. (Original) An Ethernet transceiver according to Claim 42, wherein the high attenuation is at least 20 db.

44. (Original) ~~An Ethernet transceiver according to Claim 38~~ An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a first finite impulse response filter (FIR); and

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

45. (Original) An Ethernet transceiver according to Claim 44, wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI.

46. (Amended) ~~An Ethernet transceiver according to Claim 45~~ An Ethernet transceiver, comprising:

an input circuit for inputting an input signal into an Ethernet cable;

an output circuit for outputting an output signal from the Ethernet cable, the output signal

corresponding to the input signal;

a feedforward equalizer comprising a high-pass filter and responsive to said input circuit,

wherein said high-pass filter comprises a first finite impulse response filter (FIR),

wherein said first FIR filter comprises M taps to filter precursor ISI, one main tap and N taps to filter postcursor ISI,

wherein each tap of said first FIR filter has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum_{1}^{n} W_i << 1, \text{ and}$$

$$-1 << W_1, \ldots W_n << 0; \text{ and}$$

a decision feedback equalizer comprising:

a decision circuit responsive to said feedforward equalizer; and

a feedback filter responsive to said decision circuit, wherein said decision circuit is responsive to said feedback filter.

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47. (Original) An Ethernet transceiver according to Claim 38, wherein said input circuit comprises an analog to digital converter.

48. (Original) An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a threshold circuit.

49. (Original) An Ethernet transceiver according to Claim 38, wherein said decision circuit comprises a Viterbi detector.

50. (Amended) An Ethernet transceiver according to Claim 45, further comprising ~~a first~~ an adaptive control circuit to adapt the M taps for filtering precursor ISI and N taps for filtering postcursor ISI.

51. (Original) An Ethernet transceiver according to Claim 50, wherein each of the N taps comprises a limiter to limit the range of adaptation of the N taps.

52. (Original) An Ethernet transceiver according to Claim 50, wherein said first adaptive control circuit is operable only during signal acquisition.

53. (Original) An Ethernet transceiver according to Claim 38, wherein said feedback filter comprises a second finite impulse response filter (FIR).

54. (Original) An Ethernet transceiver according to Claim 53, further comprising a second adaptive control circuit to adapt taps of said second FIR.

55. (Amended) ~~A signal processing apparatus~~ An Ethernet transceiver, comprising:

input means for receiving an input signal;

~~feedforward equalizer means for feedforward equalizing by~~ high-pass filtering means for filtering the input signal received by said input means; and

decision feedback equalizer means comprising:

decision means directly responsive to said high-pass filtering means for recovering data from an output of said ~~feedforward equalizer~~ high-pass filter means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

56. (Original) An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has a low cutoff frequency.

57. (Original) An Ethernet transceiver according to Claim 56, wherein said feedforward equalizer means has a flat response.

58. (Original) An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has high attenuation at low frequency.

59. (Original) An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means has high attenuation at low frequencies.

60. (Original) An Ethernet transceiver according to Claim. 55, wherein said feedforward equalizer means shortens a length of postcursor inter-symbol interference.

61. (Original) An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means attenuates any DC noise.

62. (Original) An Ethernet transceiver according to Claim 55, wherein said feedforward equalizer means attenuates baseline wander.

63. (Original) An Ethernet transceiver according to Claim 59, wherein the high attenuation is at least 20 db.

64. (Amended) ~~An Ethernet transceiver according to Claim 55~~ An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal; and

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

65. (Original) An Ethernet transceiver according to Claim 64, wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI.

66. (Amended) ~~An Ethernet transceiver according to Claim 65~~ An Ethernet transceiver, comprising:

input means for receiving an input signal;

feedforward equalizer means for feedforward equalizing by high-pass filtering the input signal received by said input means,

wherein said feedforward equalizer means comprises a first finite impulse response filter (FIR) means for filtering the input signal,

wherein said first FIR filter means comprises M taps for filtering precursor ISI, one main tap and N taps for filtering postcursor ISI,

wherein each tap of said first FIR filter means has a corresponding coefficient W as follows:

$$W_0 = \text{unity}$$

$$0 < \sum_{1}^{M} W_{-i} + W_o + \sum^{n} W_i << 1, \text{ and}$$

$$-1 << W_1, \ldots W_n << 0; \text{ and}$$

decision feedback equalizer means comprising:

decision means for recovering data from an output of said feedforward equalizer means; and

feedback filter means for filtering an output of said decision means, wherein said decision means is responsive to said feedback filter means.

67. (Original) An Ethernet transceiver according to Claim 55, wherein said input means comprises an analog to digital converter means for converting an analog input signal to a digital signal.

68. (Original) An Ethernet transceiver according to Claim 55, wherein said decision means comprises a threshold circuit.

69. (Original) An Ethernet transceiver according to Claim 55, wherein said decision means comprises a Viterbi detector.

70. (Amended) An Ethernet transceiver according to Claim 65, further comprising ~~a first~~ an adaptive control means for adapting the M taps for filtering precursor ISI and N taps for filtering postcursor ISI.

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71. (Original) An Ethernet transceiver according to Claim 33, wherein each of the N taps comprises a limiting means for limiting the range of adaptation of the N taps.

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72. (Original) An Ethernet transceiver according to Claim 70, wherein said first adaptive control means is operable only during signal acquisition.

73. (Original) An Ethernet transceiver according to Claim 55, wherein said feedback filter means comprises a ~~second~~ finite impulse response filter (FIR) means for filtering the output of said decision means.

74. (Original) An Ethernet transceiver according to Claim 73, further comprising ~~a second~~ an adaptive control means for adapting taps of said ~~second~~ FIR filter means.

IN THE DRAWING FIGURES:

Kindly substitute FIGS. 1-9 of the above-identified application with the enclosed six (6) replacement sheets of FIGS. 1-9, each replacement drawing sheet being identified in the top margin as "Replacement Sheet."